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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/966,954	11/10/1997	JOHANNES R. GERARDUS DE VRIES	6211P001	6312

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EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	08/966,954	GERARDUS DE VRIES, JOHANNES R.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *44-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *44-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/14/1995* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 44-50 are pending.

2. The office acknowledges the following papers:

Response to election filed on 11/4/2005,

Claims, arguments, and RCE filed on 6/27/2005.

Priority

3. The effective filing date for the subject matter defined in the pending claims in this application is 4/15/1994.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation from claim 49 "plurality of bus registers" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d).

Specification

5. The disclosure is objected to because of the following informalities:

6. The specification amendment filed on 8/26/2002 replaces section H7 of the application. However, the examiner believes the applicant deleted the incorrect

paragraph from the specification filed on 10/14/1999. It's believed that the paragraph that should have been deleted from the specification filed on 10/14/1999 is the paragraph on page 8 line 5, stating "The drive of the ..." instead of "When a clock frequency of ..." In addition, an updated specification with all of the corrects up to date would be appreciated.

7. All claimed subject matter must be contained within the specification. Thus, the limitation of claim 49 "plurality of bus registers" is not contained within the specification and must be added.

8. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The Applicant's cooperation is requested in correcting any errors of which the Applicant may become aware.

9. Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 46-47 and 49-50 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation of claim 46 "vector processing assembly code level" is unclear. The specification on page 6 lines 25-27 multiplication with 16 bit complex numbers and 8 bit vectors. For examination purposes, the limitation "vector processing assembly

code level" will be interpreted as reading on a multiply instruction. If this is the incorrect interpretation, the applicant will have to amend the specification to make mention of the correct interpretation of the limitation.

The limitation of claim 49 "plurality of bus registers" is unclear. The specification makes no mention of a bus register. It's unclear if the bus transporting data acts as a bus register or if a storage device between pipeline cycles would act as a storage device of the bus registers. For examination purposes, the "bus registers" will be interpreted as storing data in between pipeline cycles.

12. Claims 47 and 50 are rejected due to their dependency.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

14. Claims 44-50 are rejected under 35 U.S.C. §102(b) as being anticipated by Chuang (U.S. 4,766,566).

15. As per claim 44:

Chuang disclosed a processor comprising:

A plurality of functional units coupled to each other to execute operations defined from an instruction set of the processor (Chuang: Figure 7 elements 24, 60, 62, and 70, column 10 lines 18-41), the instruction set having a hierarchy of instruction levels, each of which can be used by a programmer to define instructions for the processor, the hierarchy of instruction levels including:

A RISC/CISC assembly code level (Chuang: Figure 7, column 5 lines 3-20)(The processor of figure 7 executes RISC instructions.), and

A free pipeline assembly code level (Chuang: Figure 7, column 5 lines 3-20)(In the specifications on page 3 lines 4-8, free pipeline assembly code allows the programmer to program the sequence of data flow through different execution units. RISC and CISC allow for free pipeline code. The processor of figure 7 executes RISC instructions. Thus having the same functionality.).

16. As per claim 45:

Chuang disclosed a processor as recited in claim 44, wherein the free pipeline assembly code level comprises a native machine language of the processor (Chuang: Figure 7, column 5 lines 3-20)(In the specifications on page 3 lines 4-8, free pipeline assembly code allows the programmer to program the sequence of data flow through different execution units. RISC and CISC allow for free pipeline code. The processor of figure 7 executes RISC instructions. RISC code is the native language for the processor of Chuang. Thus having the same functionality.).

17. As per claim 46:

Chuang disclosed a processor as recited in claim 44, wherein the plurality of hierarchical instruction levels further comprise a vector processing assembly code level (Chuang: Figure 7 element 24, 60, and 70, column 10 lines 18-41)(In the specifications, on page 6 lines 24-27, vectors are associated with a multiplication instruction. Chuang disclosed a multiplication instruction. Thus having the same functionality.).

18. As per claim 47:

Chuang disclosed a processor as recited in claim 46, further comprising a plurality of special use control registers, wherein the plurality of hierarchical instruction levels further comprise a level for using the special use control registers (Chuang: Figure 7 elements 44 and 46, column 5 lines 24-39 and column 10 lines 18-41).

19. As per claim 48:

Chuang disclosed a processor as recited in claim 44, wherein the plurality of functional units comprise a multiplier unit and an arithmetic logic unit (ALU), and wherein each of the plurality of functional units has an output that can be explicitly referenced in instructions defined from the instruction set (Chuang: Figure 7 elements 24, 60, 62, and 70, column 10 lines 18-41)

20. As per claim 49:

Chuang disclosed a processor as recited in claim 48, further comprising:

A plurality of dedicated output buses, one for each of the functional units (Chuang: Figure 7 element 63, column 10 lines 18-41)(Each functionality unit has an output bus to put the data on.); and

A plurality of bus registers, each coupled to store the output of only a

corresponding one of the plurality of functional units and each coupled to only a corresponding one of the plurality of dedicated output buses (Chuang: Figure 7 element 68, column 10 lines 18-41)(The output registers are coupled to the functional units and the output buses. Thus having the same functionality.).

21. As per claim 50:

Chuang disclosed a processor as recited in claim 49, wherein each of the dedicated output buses is coupled to an input of at least one other of the plurality of functional units (Chuang: Figure 7 elements 17 and 56, column 10 lines 18-41)(The bus lines are coupled to the inputs of the functional units through the register file.).

22. Claims 44 and 47-48 are rejected under 35 U.S.C. §102(e) as being anticipated by Simpson et al. (U.S. 5,487,022).

23. As per claim 44:

Simpson disclosed a processor comprising:

A plurality of functional units coupled to each other to execute operations defined from an instruction set of the processor (Simpson: Figure 12 elements 210 and 220, column 20 lines 22-41), the instruction set having a hierarchy of instruction levels, each of which can be used by a programmer to define instructions for the processor, the hierarchy of instruction levels including:

A RISC/CISC assembly code level (Simpson: Figure 3, column 11 lines 1-16)(The processor of figure 3 executes RISC instructions.), and

A free pipeline assembly code level (Simpson: Figure 3, column 11 lines 1-16)(In the specifications on page 3 lines 4-8, free pipeline assembly code allows the programmer to program the sequence of data flow through different execution units. RISC and CISC allow for free pipeline code. The processor of figure 3 executes RISC instructions. Thus having the same functionality.).

24. As per claim 46:

Simpson disclosed a processor as recited in claim 44, wherein the plurality of hierarchical instruction levels further comprise a vector processing assembly code level (Simpson: Figures 17-27, columns 25-33)(The RISC instruction set contains vector instructions.).

25. As per claim 47:

Simpson disclosed a processor as recited in claim 46, further comprising a plurality of special use control registers, wherein the plurality of hierarchical instruction levels further comprise a level for using the special use control registers (Simpson: Figure 7, column 14 lines 50-67 continued to column 15 lines 1-48)(The processor uses control registers).

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mason et al. (U.S. 5,268,855), taught a floating point ALU and multiplication functional unit executing RISC instructions

Nguyen et al. (U.S. 5,448,705), taught a RISC processor with vector instructions

Cutts, Jr. et al. (U.S. 4,965,717), taught a RISC processor with an ALU and multiplication functional units.

Nguyen et al. (U.S. 5,481,685), taught a RISC processor using control registers for ALU and multiplication functional units.

Vegesna et al. (U.S. 5,488,729), taught a RISC processor using control registers for ALU and multiplication functional units, which can execute vector instructions.

Hinton et al. (U.S. Statutory Invention Registration H1291), taught a RISC processor using control registers for ALU and multiplication functional units.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner
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